



128K x 32, 128K x 36, 256K x 18 4 Mb SYNCHRONOUS PIPELINED, SINGLE CYCLE DESELECT STATIC RAM

APRIL 2008

FEATURES

- Internal self-timed write cycle
- Individual Byte Write Control and Global Write
- Clock controlled, registered address, data and control
- Burst sequence control using MODE input
- Three chip enable option for simple depth expansion and address pipelining
- Common data inputs and data outputs
- Auto Power-down during deselect
- Single cycle deselect
- Snooze MODE for reduced-power standby
- Power Supply
LPS: $V_{DD} 3.3V \pm 5\%$, $V_{DDQ} 3.3V/2.5V \pm 5\%$
VPS: $V_{DD} 2.5V \pm 5\%$, $V_{DDQ} 2.5V \pm 5\%$
- JEDEC 100-Pin TQFP, 119-ball PBGA, and 165-ball PBGA packages
- Automotive temperature available
- Lead Free available

DESCRIPTION

The *ISSI* IS61(64)LPS12832A, IS61(64)LPS/VPS12836A and IS61(64)LPS/VPS25618A are high-speed, low-power synchronous static RAMs designed to provide burstable, high-performance memory for communication and networking applications. The IS61(64)LPS12832A is organized as 131,072 words by 32 bits. The IS61(64)LPS/VPS12836A is organized as 131,072 words by 36 bits. The IS61(64)LPS/VPS25618A is organized as 262,144 words by 18 bits. Fabricated with *ISSI*'s advanced CMOS technology, the device integrates a 2-bit burst counter, high-speed SRAM core, and high-drive capability outputs into a single monolithic circuit. All synchronous inputs pass through registers controlled by a positive-edge-triggered single clock input.

Write cycles are internally self-timed and are initiated by the rising edge of the clock input. Write cycles can be one to four bytes wide as controlled by the write control inputs.

Separate byte enables allow individual bytes to be written. The byte write operation is performed by using the byte write enable (\overline{BWE}) input combined with one or more individual byte write signals (\overline{BWx}). In addition, Global Write (\overline{GW}) is available for writing all bytes at one time, regardless of the byte write controls.

Bursts can be initiated with either \overline{ADSP} (Address Status Processor) or \overline{ADSC} (Address Status Cache Controller) input pins. Subsequent burst addresses can be generated internally and controlled by the \overline{ADV} (burst address advance) input pin.

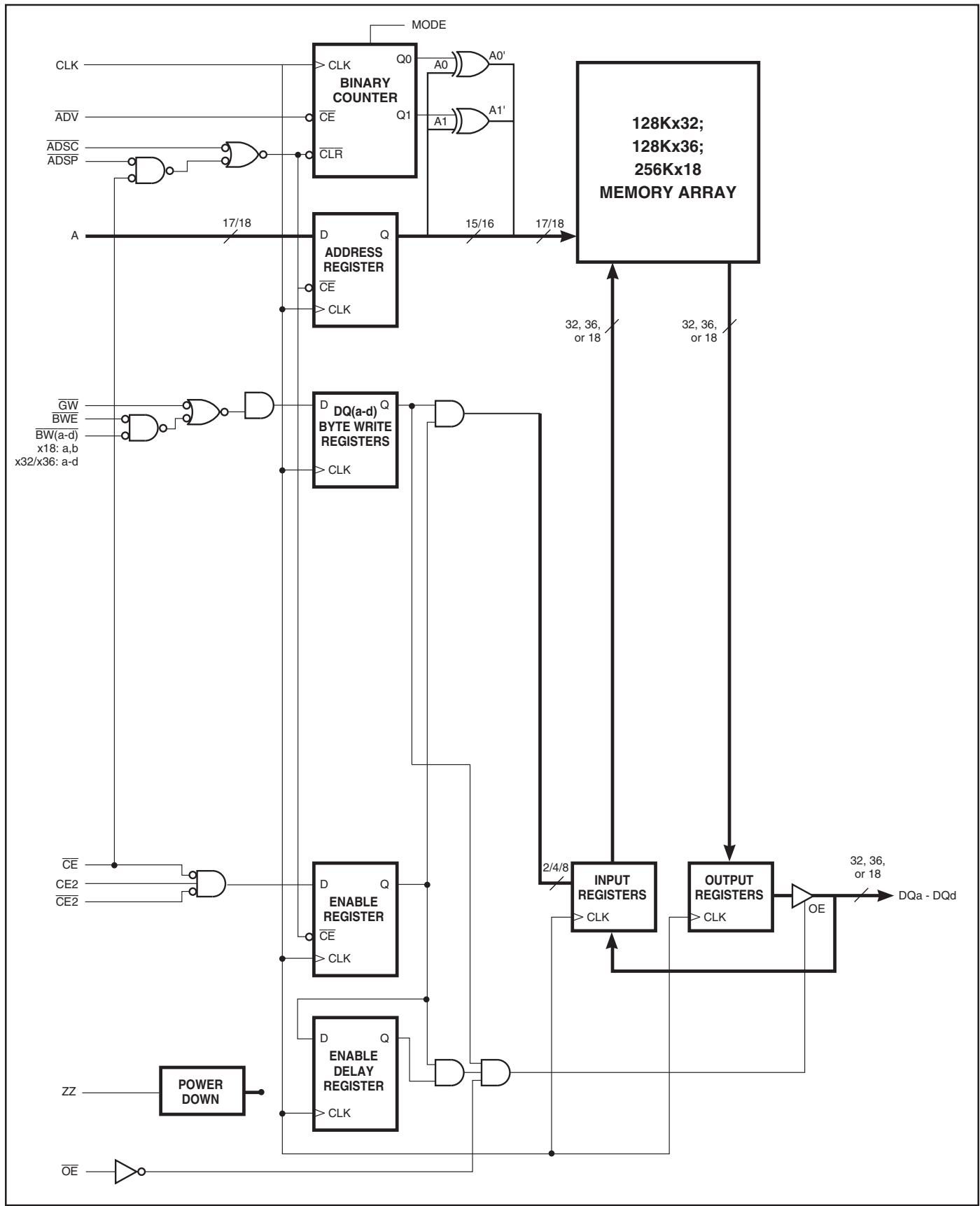
The mode pin is used to select the burst sequence order, Linear burst is achieved when this pin is tied LOW. Interleave burst is achieved when this pin is tied HIGH or left floating.

FAST ACCESS TIME

| Symbol | Parameter | 250 | 200 | Units |
|--------|-------------------|-----|-----|-------|
| tkQ | Clock Access Time | 2.6 | 3.1 | ns |
| tkC | Cycle Time | 4 | 5 | ns |
| | Frequency | 250 | 200 | MHz |

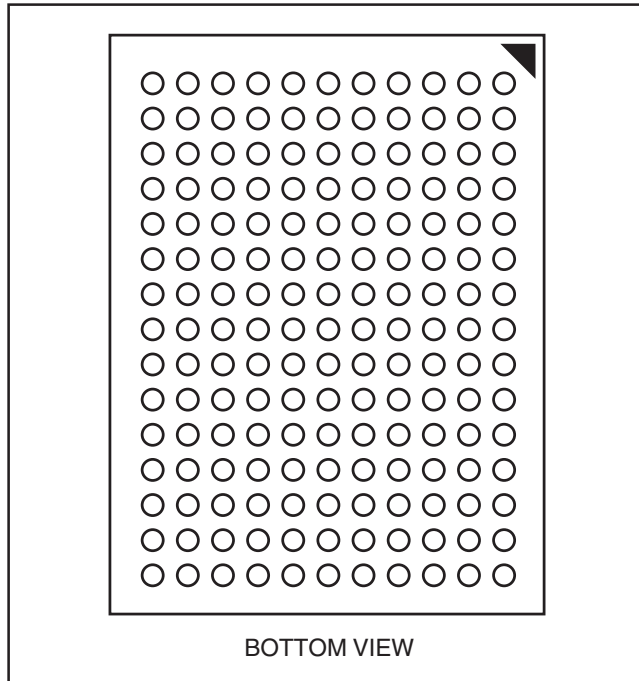
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BLOCK DIAGRAM



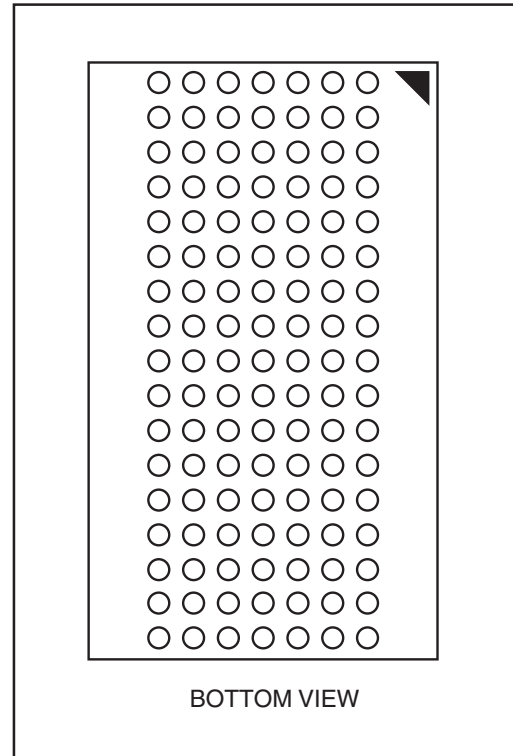
165-PIN BGA

165-Ball, 13x15 mm BGA
1mm Ball Pitch, 11x15 Ball Array



119-PIN BGA

119-Ball, 14x22 mm BGA
1mm Ball Pitch, 7x17 Ball Array



119 BGA PACKAGE PIN CONFIGURATION

128K x 36 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|----------|------------------|-----------------|-------------------------|--------------------------|-------------------------|-------------------------|------------------|
| A | V _{DDQ} | A | A | $\overline{\text{ADSP}}$ | A | A | V _{DDQ} |
| B | NC | CE2 | A | $\overline{\text{ADSC}}$ | A | $\overline{\text{CE2}}$ | NC |
| C | NC | A | A | V _{DD} | A | A | NC |
| D | DQc | DQPc | V _{SS} | NC | V _{SS} | DQPb | DQb |
| E | DQc | DQc | V _{SS} | $\overline{\text{CE}}$ | V _{SS} | DQb | DQb |
| F | V _{DDQ} | DQc | V _{SS} | $\overline{\text{OE}}$ | V _{SS} | DQb | V _{DDQ} |
| G | DQc | DQc | $\overline{\text{BWC}}$ | $\overline{\text{ADV}}$ | $\overline{\text{BWb}}$ | DQb | DQb |
| H | DQc | DQc | V _{SS} | $\overline{\text{GW}}$ | V _{SS} | DQb | DQb |
| J | V _{DDQ} | V _{DD} | NC | V _{DD} | NC | V _{DD} | V _{DDQ} |
| K | DQd | DQd | V _{SS} | CLK | V _{SS} | DQa | DQa |
| L | DQd | DQd | $\overline{\text{BWD}}$ | NC | $\overline{\text{BWA}}$ | DQa | DQa |
| M | V _{DDQ} | DQd | V _{SS} | $\overline{\text{BWE}}$ | V _{SS} | DQa | V _{DDQ} |
| N | DQd | DQd | V _{SS} | A ₁ * | V _{SS} | DQa | DQa |
| P | DQd | DQPd | V _{SS} | A ₀ * | V _{SS} | DQPa | DQa |
| R | NC | A | MODE | V _{DD} | NC | A | NC |
| T | NC | NC | A | A | A | NC | ZZ |
| U | V _{DDQ} | NC | NC | NC | NC | NC | V _{DDQ} |

Note: * A₀ and A₁ are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

| Symbol | Pin Name |
|---|-----------------------------------|
| A | Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| $\overline{\text{ADV}}$ | Synchronous Burst Address Advance |
| $\overline{\text{ADSP}}$ | Address Status Processor |
| $\overline{\text{ADSC}}$ | Address Status Controller |
| $\overline{\text{GW}}$ | Global Write Enable |
| CLK | Synchronous Clock |
| $\overline{\text{CE}}$, CE2, $\overline{\text{CE2}}$ | Synchronous Chip Select |
| $\overline{\text{BW}}_x$ (x=a-d) | Synchronous Byte Write Controls |
| $\overline{\text{BWE}}$ | Byte Write Enable |

| Symbol | Pin Name |
|------------------------|--------------------------|
| $\overline{\text{OE}}$ | Output Enable |
| ZZ | Power Sleep Mode |
| MODE | Burst Sequence Selection |
| NC | No Connect |
| DQa-DQd | Data Inputs/Outputs |
| DQPa-Pd | Output Power Supply |
| V _{DD} | Power Supply |
| V _{DDQ} | Output Power Supply |
| V _{SS} | Ground |

119 BGA PACKAGE PIN CONFIGURATION

256Kx18 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 |
|----------|------------------|------------------|-------------------------|--------------------------|-------------------------|-------------------------|------------------|
| A | V _{DDQ} | A | A | $\overline{\text{ADSP}}$ | A | A | V _{DDQ} |
| B | NC | CE2 | A | $\overline{\text{ADSC}}$ | A | $\overline{\text{CE2}}$ | NC |
| C | NC | A | A | V _{DD} | A | A | NC |
| D | DQ _b | NC | V _{SS} | NC | V _{SS} | DQP _a | NC |
| E | NC | DQ _b | V _{SS} | $\overline{\text{CE}}$ | V _{SS} | NC | DQ _a |
| F | V _{DDQ} | NC | V _{SS} | $\overline{\text{OE}}$ | V _{SS} | DQ _a | V _{DDQ} |
| G | NC | DQ _b | $\overline{\text{Bwb}}$ | $\overline{\text{ADV}}$ | V _{SS} | NC | DQ _a |
| H | DQ _b | NC | V _{SS} | $\overline{\text{GW}}$ | V _{SS} | DQ _a | NC |
| J | V _{DDQ} | V _{DD} | NC | V _{DD} | NC | V _{DD} | V _{DDQ} |
| K | NC | DQ _b | V _{SS} | CLK | V _{SS} | NC | DQ _a |
| L | DQ _b | NC | V _{SS} | NC | $\overline{\text{Bwa}}$ | DQ _a | NC |
| M | V _{DDQ} | DQ _b | V _{SS} | $\overline{\text{BWE}}$ | V _{SS} | NC | V _{DDQ} |
| N | DQ _b | NC | V _{SS} | A ₁ * | V _{SS} | DQ _a | NC |
| P | NC | DQP _b | V _{SS} | A ₀ * | V _{SS} | NC | DQ _a |
| R | NC | A | MODE | V _{DD} | NC | A | NC |
| T | NC | A | A | NC | A | A | ZZ |
| U | V _{DDQ} | NC | NC | NC | NC | NC | V _{DDQ} |

Note: * A₀ and A₁ are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

| Symbol | Pin Name |
|---|-----------------------------------|
| A | Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| $\overline{\text{ADV}}$ | Synchronous Burst Address Advance |
| $\overline{\text{ADSP}}$ | Address Status Processor |
| $\overline{\text{ADSC}}$ | Address Status Controller |
| $\overline{\text{GW}}$ | Global Write Enable |
| CLK | Synchronous Clock |
| $\overline{\text{CE}}$, CE2, $\overline{\text{CE2}}$ | Synchronous Chip Select |
| $\overline{\text{BW}}_x$ (x=a,b) | Synchronous Byte Write Controls |
| $\overline{\text{BWE}}$ | Byte Write Enable |

| Symbol | Pin Name |
|----------------------------------|--------------------------|
| $\overline{\text{OE}}$ | Output Enable |
| ZZ | Power Sleep Mode |
| MODE | Burst Sequence Selection |
| NC | No Connect |
| DQ _a -DQ _b | Data Inputs/Outputs |
| DQP _a -P _b | Output Power Supply |
| V _{DD} | Power Supply |
| V _{DDQ} | Output Power Supply |
| V _{SS} | Ground |



165 PBGA PACKAGE PIN CONFIGURATION

128K x 36 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|----------|------|-----|-----------------|------------------|------------------|------------------|------------------|-------------------|-------------------|-----|------|
| A | NC | A | \overline{CE} | \overline{BWc} | \overline{BWb} | $\overline{CE2}$ | \overline{BWE} | \overline{ADSC} | \overline{ADV} | A | NC |
| B | NC | A | CE2 | \overline{BWd} | \overline{BWa} | CLK | \overline{GW} | \overline{OE} | \overline{ADSP} | A | NC |
| C | DQPc | NC | VDDQ | VSS | VSS | VSS | VSS | VSS | VDDQ | NC | DQPb |
| D | DQc | DQc | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | DQb | DQb |
| E | DQc | DQc | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | DQb | DQb |
| F | DQc | DQc | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | DQb | DQb |
| G | DQc | DQc | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | DQb | DQb |
| H | NC | NC | NC | VDD | VSS | VSS | VSS | VDD | NC | NC | ZZ |
| J | DQd | DQd | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | DQa | DQa |
| K | DQd | DQd | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | DQa | DQa |
| L | DQd | DQd | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | DQa | DQa |
| M | DQd | DQd | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | DQa | DQa |
| N | DQPd | NC | VDDQ | VSS | NC | NC | NC | VSS | VDDQ | NC | DQPd |
| P | NC | NC | A | A | NC | A1* | NC | A | A | A | NC |
| R | MODE | NC | A | A | NC | A0* | NC | A | A | A | A |

Note: * A0 and A1 are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

| Symbol | Pin Name |
|--|-----------------------------------|
| A | Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| \overline{ADV} | Synchronous Burst Address Advance |
| \overline{ADSP} | Address Status Processor |
| \overline{ADSC} | Address Status Controller |
| \overline{GW} | Global Write Enable |
| CLK | Synchronous Clock |
| \overline{CE} , $\overline{CE2}$, CE2 | Synchronous Chip Select |
| \overline{BWx} (x=a,b,c,d) | Synchronous Byte Write Controls |

| Symbol | Pin Name |
|------------------|---|
| \overline{BWE} | Byte Write Enable |
| \overline{OE} | Output Enable |
| ZZ | Power Sleep Mode |
| MODE | Burst Sequence Selection |
| NC | No Connect |
| DQx | Data Inputs/Outputs |
| DQPx | Data Inputs/Outputs |
| VDD | 3.3V/2.5V Power Supply |
| VDDQ | Isolated Output Power Supply 3.3V/2.5V |
| VSS | Ground |

165 PBGA PACKAGE PIN CONFIGURATION

256K x 18 (TOP VIEW)

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 |
|----------|------------------|-----------------|-----------------|------------------|------------------|------------------|------------------|-------------------|-------------------|-----------------|------------------|
| A | NC | A | \overline{CE} | \overline{BWb} | NC | $\overline{CE2}$ | \overline{BWE} | \overline{ADSC} | \overline{ADV} | A | A |
| B | NC | A | CE2 | NC | \overline{Bwa} | CLK | \overline{GW} | \overline{OE} | \overline{ADSP} | A | NC |
| C | NC | NC | VDDQ | VSS | VSS | VSS | VSS | VSS | VDDQ | NC | DQP _a |
| D | NC | DQ _b | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | DQ _a |
| E | NC | DQ _b | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | DQ _a |
| F | NC | DQ _b | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | DQ _a |
| G | NC | DQ _b | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | NC | DQ _a |
| H | NC | NC | NC | VDD | VSS | VSS | VSS | VDD | NC | NC | ZZ |
| J | DQ _b | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | DQ _a | NC |
| K | DQ _b | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | DQ _a | NC |
| L | DQ _b | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | DQ _a | NC |
| M | DQ _b | NC | VDDQ | VDD | VSS | VSS | VSS | VDD | VDDQ | DQ _a | NC |
| N | DQP _b | NC | VDDQ | VSS | NC | NC | NC | VSS | VDDQ | NC | NC |
| P | NC | NC | A | A | NC | A1* | NC | A | A | A | NC |
| R | MODE | NC | A | A | NC | A0* | NC | A | A | A | A |

Note: * A₀ and A₁ are the two least significant bits (LSB) of the address field and set the internal burst counter if burst is desired.

PIN DESCRIPTIONS

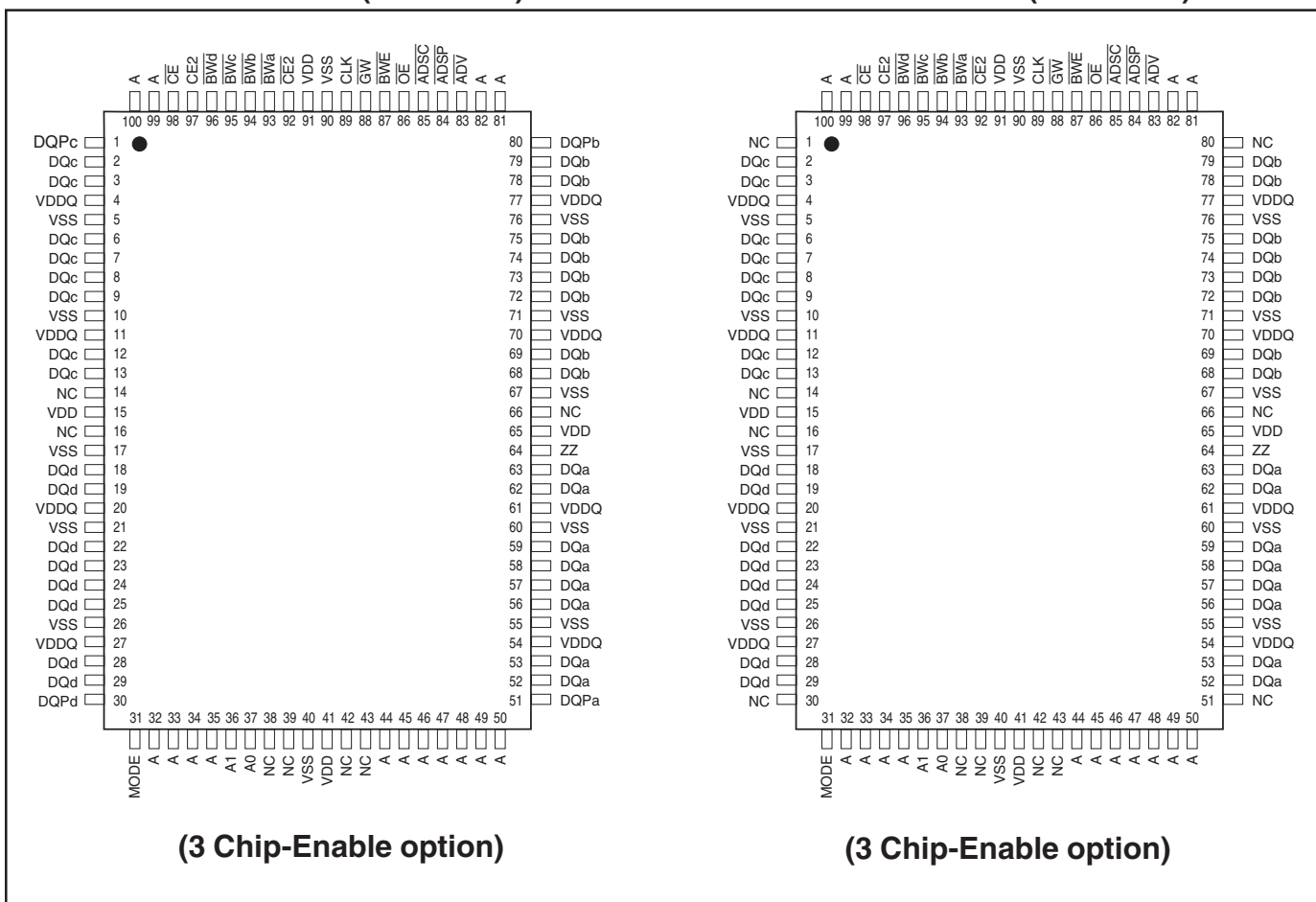
| Symbol | Pin Name |
|--|-----------------------------------|
| A | Address Inputs |
| A0, A1 | Synchronous Burst Address Inputs |
| \overline{ADV} | Synchronous Burst Address Advance |
| \overline{ADSP} | Address Status Processor |
| \overline{ADSC} | Address Status Controller |
| \overline{GW} | Global Write Enable |
| CLK | Synchronous Clock |
| \overline{CE} , $\overline{CE2}$, CE2 | Synchronous Chip Select |
| \overline{BWx} (x=a,b) | Synchronous Byte Write Controls |

| Symbol | Pin Name |
|------------------|---|
| \overline{BWE} | Byte Write Enable |
| \overline{OE} | Output Enable |
| ZZ | Power Sleep Mode |
| MODE | Burst Sequence Selection |
| NC | No Connect |
| DQ _x | Data Inputs/Outputs |
| DQP _x | Data Inputs/Outputs |
| VDD | 3.3V/2.5V Power Supply |
| VDDQ | Isolated Output Power Supply 3.3V/2.5V |
| VSS | Ground |

PIN CONFIGURATION

100-PIN TQFP (128K X 36)

100-PIN TQFP (128K X 32)



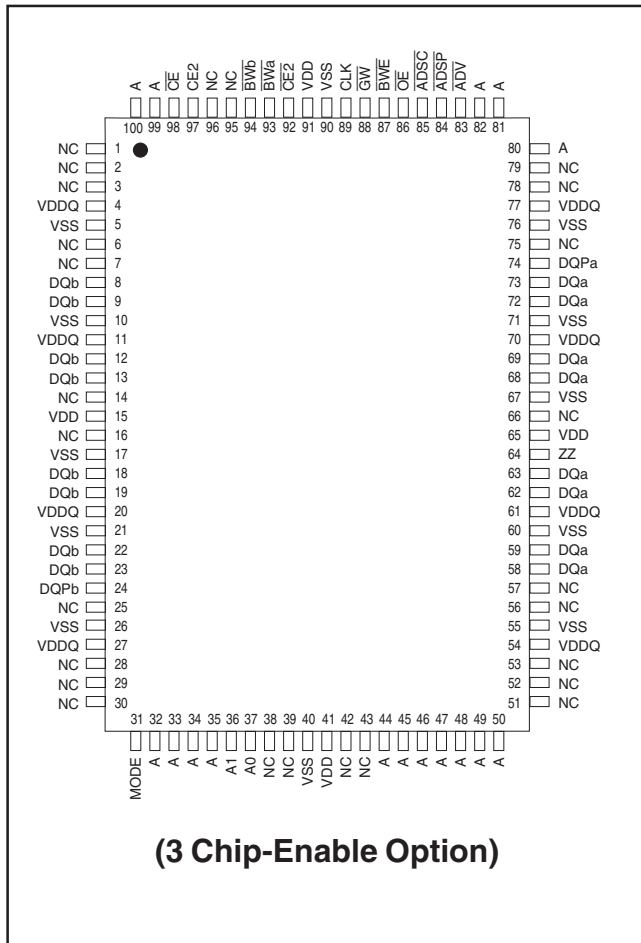
PIN DESCRIPTIONS

| | |
|--|--|
| A0, A1 | Synchronous Address Inputs. These pins must tied to the two LSBs of the address bus. |
| A | Synchronous Address Inputs |
| $\overline{\text{ADSC}}$ | Synchronous Controller Address Status |
| $\overline{\text{ADSP}}$ | Synchronous Processor Address Status |
| $\overline{\text{ADV}}$ | Synchronous Burst Address Advance |
| $\overline{\text{BWA}}\text{-}\overline{\text{BWd}}$ | Synchronous Byte Write Enable |
| $\overline{\text{BWE}}$ | Synchronous Byte Write Enable |
| $\overline{\text{CE}}$, $\overline{\text{CE2}}$, CE2 | Synchronous Chip Enable |
| CLK | Synchronous Clock |

| | |
|------------------------|---|
| DQa-DQd | Synchronous Data Input/Output |
| DQPa-DQPd | Parity Data Input/Output |
| $\overline{\text{GW}}$ | Synchronous Global Write Enable |
| MODE | Burst Sequence Mode Selection |
| $\overline{\text{OE}}$ | Output Enable |
| VDD | 3.3V/2.5V Power Supply |
| VDDQ | Isolated Output Buffer Supply: 3.3V/2.5V |
| VSS | Ground |
| ZZ | Snooze Enable |

PIN CONFIGURATION

100-PIN TQFP (256K X 18)



PIN DESCRIPTIONS

| | | | |
|---|---|------------------------------------|---|
| A0, A1 | Synchronous Address Inputs. These pins must be tied to the two LSBs of the address bus. | DQP _a -DQP _b | Parity Data I/O; DQP _a is parity for DQ _a 1-8; DQP _b is parity for DQ _b 1-8 |
| A | Synchronous Address Inputs | \overline{GW} | Synchronous Global Write Enable |
| \overline{ADSC} | Synchronous Controller Address Status | MODE | Burst Sequence Mode Selection |
| \overline{ADSP} | Synchronous Processor Address Status | \overline{OE} | Output Enable |
| \overline{ADV} | Synchronous Burst Address Advance | V _{DD} | 3.3V/2.5V Power Supply |
| \overline{BWA} - \overline{BWB} | Synchronous Byte Write Enable | V _{DDQ} | Isolated Output Buffer Supply: 3.3V/2.5V |
| \overline{BWE} | Synchronous Byte Write Enable | V _{SS} | Ground |
| \overline{CE} , CE2, $\overline{CE2}$ | Synchronous Chip Enable | \overline{ZZ} | Snooze Enable |
| CLK | Synchronous Clock | | |
| DQ _a -DQ _b | Synchronous Data Input/Output | | |



TRUTH TABLE⁽¹⁻⁸⁾

| OPERATION | ADDRESS | \overline{CE} | $\overline{CE2}$ | CE2 | ZZ | \overline{ADSP} | \overline{ADSC} | \overline{ADV} | WRITE | \overline{OE} | CLK | DQ |
|-----------------------------|----------|-----------------|------------------|-----|----|-------------------|-------------------|------------------|-------|-----------------|-----|--------|
| Deselect Cycle, Power-Down | None | H | X | X | L | X | L | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | X | L | L | L | X | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | H | X | L | L | X | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | X | L | L | H | L | X | X | X | L-H | High-Z |
| Deselect Cycle, Power-Down | None | L | H | X | L | H | L | X | X | X | L-H | High-Z |
| Snooze Mode, Power-Down | None | X | X | X | H | X | X | X | X | X | X | High-Z |
| Read Cycle, Begin Burst | External | L | L | H | L | L | X | X | X | L | L-H | Q |
| Read Cycle, Begin Burst | External | L | L | H | L | L | X | X | X | H | L-H | High-Z |
| Write Cycle, Begin Burst | External | L | L | H | L | H | L | X | L | X | L-H | D |
| Read Cycle, Begin Burst | External | L | L | H | L | H | L | X | H | L | L-H | Q |
| Read Cycle, Begin Burst | External | L | L | H | L | H | L | X | H | H | L-H | High-Z |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | L | L-H | Q |
| Read Cycle, Continue Burst | Next | X | X | X | L | H | H | L | H | H | L-H | High-Z |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | L | L-H | Q |
| Read Cycle, Continue Burst | Next | H | X | X | L | X | H | L | H | H | L-H | High-Z |
| Write Cycle, Continue Burst | Next | X | X | X | L | H | H | L | L | X | L-H | D |
| Write Cycle, Continue Burst | Next | H | X | X | L | X | H | L | L | X | L-H | D |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | L | L-H | Q |
| Read Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | H | H | L-H | High-Z |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | L | L-H | Q |
| Read Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | H | H | L-H | High-Z |
| Write Cycle, Suspend Burst | Current | X | X | X | L | H | H | H | L | X | L-H | D |
| Write Cycle, Suspend Burst | Current | H | X | X | L | X | H | H | L | X | L-H | D |

NOTE:

1. X means "Don't Care." H means logic HIGH. L means logic LOW.
2. For **WRITE**, L means one or more byte write enable signals ($\overline{BWA-d}$) and \overline{BWE} are LOW or \overline{GW} is LOW. **WRITE** = H for all \overline{BWx} , \overline{BWE} , \overline{GW} HIGH.
3. \overline{BWA} enables WRITES to DQa's and DQPa. \overline{BWb} enables WRITES to DQb's and DQPb. \overline{BWC} enables WRITES to DQc's and DQPC. \overline{BWD} enables WRITES to DQd's and DQPd. DQPa and DQPb are available on the x18 version. DQPa-DQPd are available on the x36 version.
4. All inputs except \overline{OE} and ZZ must meet setup and hold times around the rising edge (LOW to HIGH) of CLK.
5. Wait states are inserted by suspending burst.
6. For a WRITE operation following a READ operation, \overline{OE} must be HIGH before the input data setup time and held HIGH during the input data hold time.
7. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.
8. \overline{ADSP} LOW always initiates an internal READ at the L-H edge of CLK. A WRITE is performed by setting one or more byte write enable signals and \overline{BWE} LOW or \overline{GW} LOW for the subsequent L-H edge of CLK. See WRITE timing diagram for clarification.

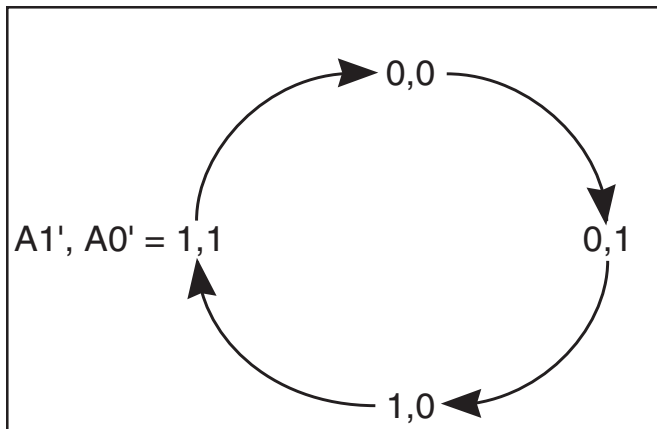
PARTIAL TRUTH TABLE

| Function | \overline{GW} | \overline{BWE} | \overline{BWA} | \overline{BWb} | \overline{BWC} | \overline{BWD} |
|-----------------|-----------------|------------------|------------------|------------------|------------------|------------------|
| Read | H | H | X | X | X | X |
| Read | H | L | H | H | H | H |
| Write Byte 1 | H | L | L | H | H | H |
| Write All Bytes | H | L | L | L | L | L |
| Write All Bytes | L | X | X | X | X | X |

INTERLEAVED BURST ADDRESS TABLE (MODE = V_{DD} or No Connect)

| External Address A1 A0 | 1st Burst Address A1 A0 | 2nd Burst Address A1 A0 | 3rd Burst Address A1 A0 |
|---------------------------|----------------------------|----------------------------|----------------------------|
| 00 | 01 | 10 | 11 |
| 01 | 00 | 11 | 10 |
| 10 | 11 | 00 | 01 |
| 11 | 10 | 01 | 00 |

LINEAR BURST ADDRESS TABLE (MODE = V_{SS})



ABSOLUTE MAXIMUM RATINGS⁽¹⁾

| Symbol | Parameter | Value | Unit |
|------------------------------------|---|--------------------------------|------|
| T _{STG} | Storage Temperature | -55 to +150 | °C |
| P _D | Power Dissipation | 1.6 | W |
| I _{OUT} | Output Current (per I/O) | 100 | mA |
| V _{IN} , V _{OUT} | Voltage Relative to V _{SS} for I/O Pins | -0.5 to V _{DDQ} + 0.5 | V |
| V _{IN} | Voltage Relative to V _{SS} for for Address and Control Inputs | -0.5 to V _{DD} + 0.5 | V |
| V _{DD} | Voltage on V _{DD} Supply Relative to V _{SS} | -0.5 to 4.6 | V |

Notes:

1. Stress greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, precautions may be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.
3. This device contains circuitry that will ensure the output devices are in High-Z at power up.

OPERATING RANGE (IS61/64LPSXXXXX)

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|---------------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |
| Industrial | -40°C to +85°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |
| Automotive | -40°C to +125°C | 3.3V ± 5% | 3.3V / 2.5V ± 5% |

OPERATING RANGE (IS61/64VPSXXXXX)

| Range | Ambient Temperature | V _{DD} | V _{DDQ} |
|------------|---------------------|-----------------|------------------|
| Commercial | 0°C to +70°C | 2.5V ± 5% | 2.5V ± 5% |
| Industrial | -40°C to +85°C | 2.5V ± 5% | 2.5V ± 5% |
| Automotive | -40°C to +125°C | 2.5V ± 5% | 2.5V ± 5% |

DC ELECTRICAL CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | Test Conditions | 3.3V | | 2.5V | | Unit |
|-----------------|------------------------|---|------|-----------------------|------|-----------------------|------|
| | | | Min. | Max. | Min. | Max. | |
| V _{OH} | Output HIGH Voltage | I _{OH} = -4.0 mA (3.3V) I _{OH} = -1.0 mA (2.5V) | 2.4 | — | 2.0 | — | V |
| V _{OL} | Output LOW Voltage | I _{OL} = 8.0 mA (3.3V) I _{OL} = 1.0 mA (2.5V) | — | 0.4 | — | 0.4 | V |
| V _{IH} | Input HIGH Voltage | | 2.0 | V _{DD} + 0.3 | 1.7 | V _{DD} + 0.3 | V |
| V _{IL} | Input LOW Voltage | | -0.3 | 0.8 | -0.3 | 0.7 | V |
| I _{LI} | Input Leakage Current | V _{SS} ≤ V _{IN} ≤ V _{DD} ⁽¹⁾ | -5 | 5 | -5 | 5 | μA |
| I _{LO} | Output Leakage Current | V _{SS} ≤ V _{OUT} ≤ V _{DDQ} , $\overline{OE} = V_{IH}$ | -5 | 5 | -5 | 5 | μA |

POWER SUPPLY CHARACTERISTICS⁽¹⁾ (Over Operating Range)

| Symbol | Parameter | Test Conditions | Temp. range | -250 MAX | | -200 MAX | | Unit |
|------------------|--------------------------------|---|---------------------|-------------|---------|-------------|---------|------|
| | | | | x18 | x32/x36 | x18 | x32/x36 | |
| I _{CC} | AC Operating Supply Current | Device Selected, $\overline{OE} = V_{IH}$, $ZZ \leq V_{IL}$, All Inputs $\leq 0.2V$ or $\geq V_{DD} - 0.2V$, Cycle Time $\geq t_{kc}$ min. | Com. | 225 | 225 | 200 | 200 | mA |
| | | | Ind. | 250 | 250 | 210 | 210 | |
| | | | Auto. | 275 | 275 | 225 | 225 | |
| I _{SB} | Standby Current TTL Input | Device Deselected, $V_{DD} = \text{Max.}$, All Inputs $\leq V_{IL}$ or $\geq V_{IH}$, $ZZ \leq V_{IL}$, $f = \text{Max.}$ | Com. | 90 | 90 | 90 | 90 | mA |
| | | | Ind. | 100 | 100 | 100 | 100 | |
| | | | Auto. | 120 | 120 | 120 | 120 | |
| I _{SBI} | Standby Current CMOS Input | Device Deselected, $V_{DD} = \text{Max.}$, $V_{IN} \leq V_{SS} + 0.2V$ or $\geq V_{DD} - 0.2V$ $f = 0$ | Com. | 70 | 70 | 70 | 70 | mA |
| | | | Ind. | 75 | 75 | 75 | 75 | |
| | | | Auto. | 90 | 90 | 90 | 90 | |
| | | | typ. ⁽²⁾ | 40 | | 40 | | |

Note:

1. MODE pin has an internal pullup and should be tied to V_{DD} or V_{SS} . It exhibits $\pm 100\mu A$ maximum leakage current when tied to $\leq V_{SS} + 0.2V$ or $\geq V_{DD} - 0.2V$.
2. Typical values are measured at $V_{DD} = 3.3V$, $T_A = 25^\circ C$ and not 100% tested.

CAPACITANCE^(1,2)

| Symbol | Parameter | Conditions | Max. | Unit |
|------------------|--------------------------|-----------------------|------|------|
| C _{IN} | Input Capacitance | V _{IN} = 0V | 6 | pF |
| C _{OUT} | Input/Output Capacitance | V _{OUT} = 0V | 8 | pF |

Notes:

1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1 MHz, V_{DD} = 3.3V.

3.3V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 3.0V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

AC TEST LOADS

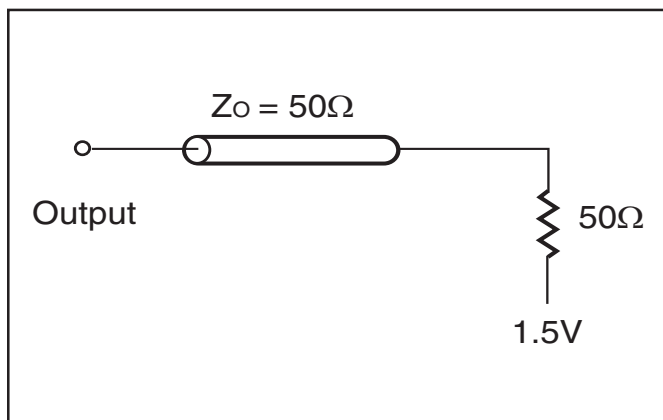


Figure 1

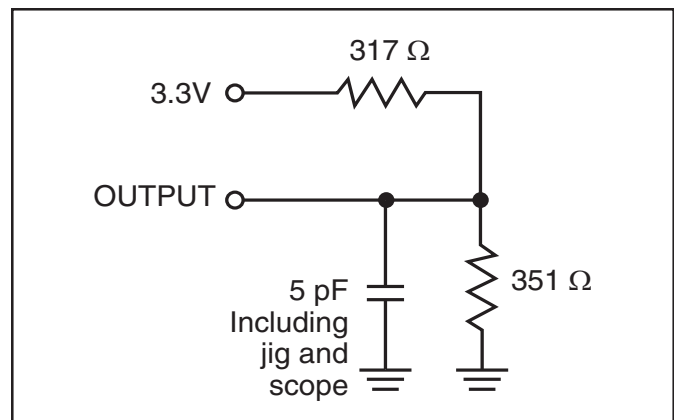


Figure 2

2.5V I/O AC TEST CONDITIONS

| Parameter | Unit |
|---|---------------------|
| Input Pulse Level | 0V to 2.5V |
| Input Rise and Fall Times | 1.5 ns |
| Input and Output Timing and Reference Level | 1.25V |
| Output Load | See Figures 3 and 4 |

2.5 I/O OUTPUT LOAD EQUIVALENT

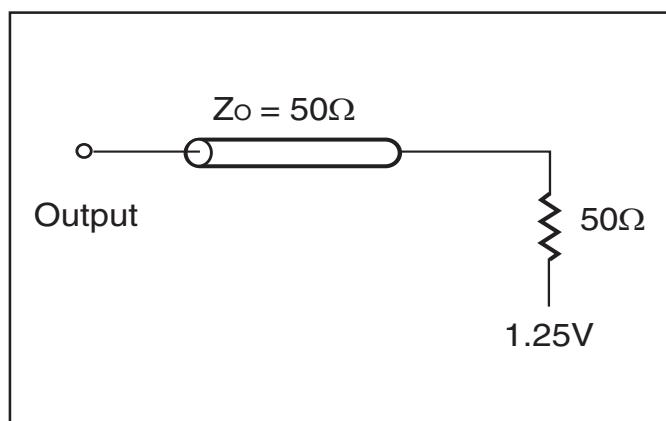


Figure 3

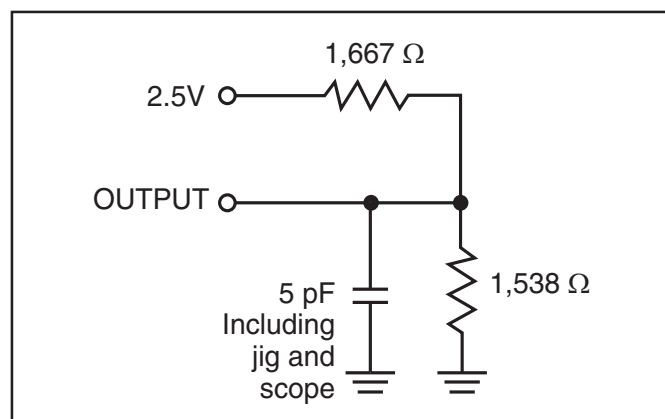


Figure 4

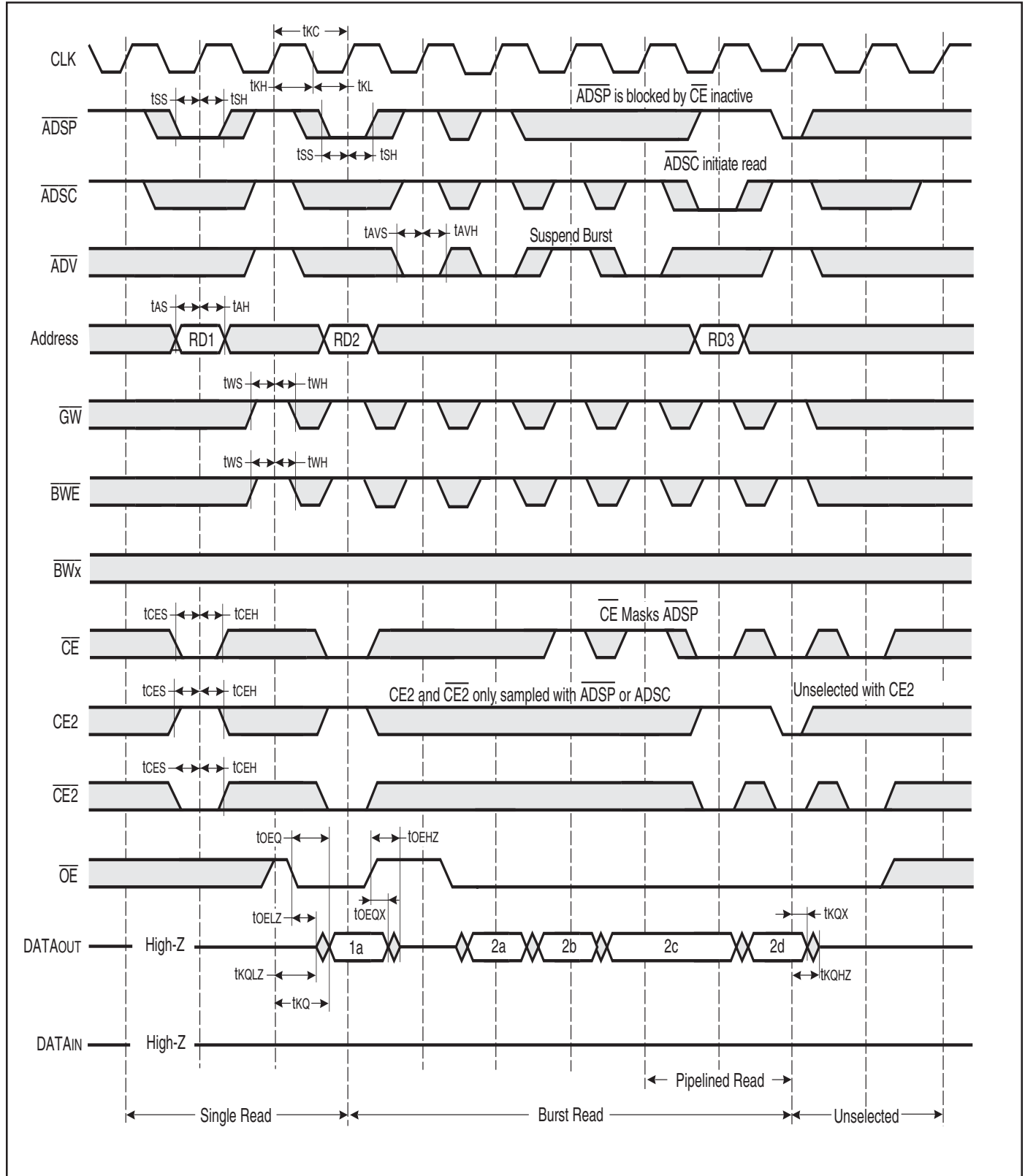
READ/WRITE CYCLE SWITCHING CHARACTERISTICS (Over Operating Range)

| Symbol | Parameter | -250 | | -200 | | Unit |
|------------------------------------|----------------------------------|------|------|------|------|------|
| | | Min. | Max. | Min. | Max. | |
| f _{MAX} | Clock Frequency | — | 250 | — | 200 | MHz |
| t _{KC} | Cycle Time | 4.0 | — | 5 | — | ns |
| t _{KH} | Clock High Time | 1.7 | — | 2 | — | ns |
| t _{KL} | Clock Low Time | 1.7 | — | 2 | — | ns |
| t _{KQ} | Clock Access Time | — | 2.6 | — | 3.1 | ns |
| t _{KQX} ⁽²⁾ | Clock High to Output Invalid | 0.8 | — | 1.5 | — | ns |
| t _{KQLZ} ^(2,3) | Clock High to Output Low-Z | 0.8 | — | 1 | — | ns |
| t _{KQHZ} ^(2,3) | Clock High to Output High-Z | — | 2.6 | — | 3.0 | ns |
| t _{OEQ} | Output Enable to Output Valid | — | 2.8 | — | 3.1 | ns |
| t _{OEQX} ⁽²⁾ | Output Disable to Output Invalid | 0 | — | 0 | — | ns |
| t _{OELZ} ^(2,3) | Output Enable to Output Low-Z | 0 | — | 0 | — | ns |
| t _{OEHZ} ^(2,3) | Output Disable to Output High-Z | — | 2.6 | — | 3.0 | ns |
| t _{AS} | Address Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{SS} | Address Status Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{WS} | Read/Write Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{CES} | Chip Enable Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{AVS} | Address Advance Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{DS} | Data Setup Time | 1.2 | — | 1.4 | — | ns |
| t _{AH} | Address Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{SH} | Address Status Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{WH} | Write Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{CEH} | Chip Enable Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{AVH} | Address Advance Hold Time | 0.3 | — | 0.4 | — | ns |
| t _{DH} | Data Hold Time | 0.3 | — | 0.4 | — | ns |

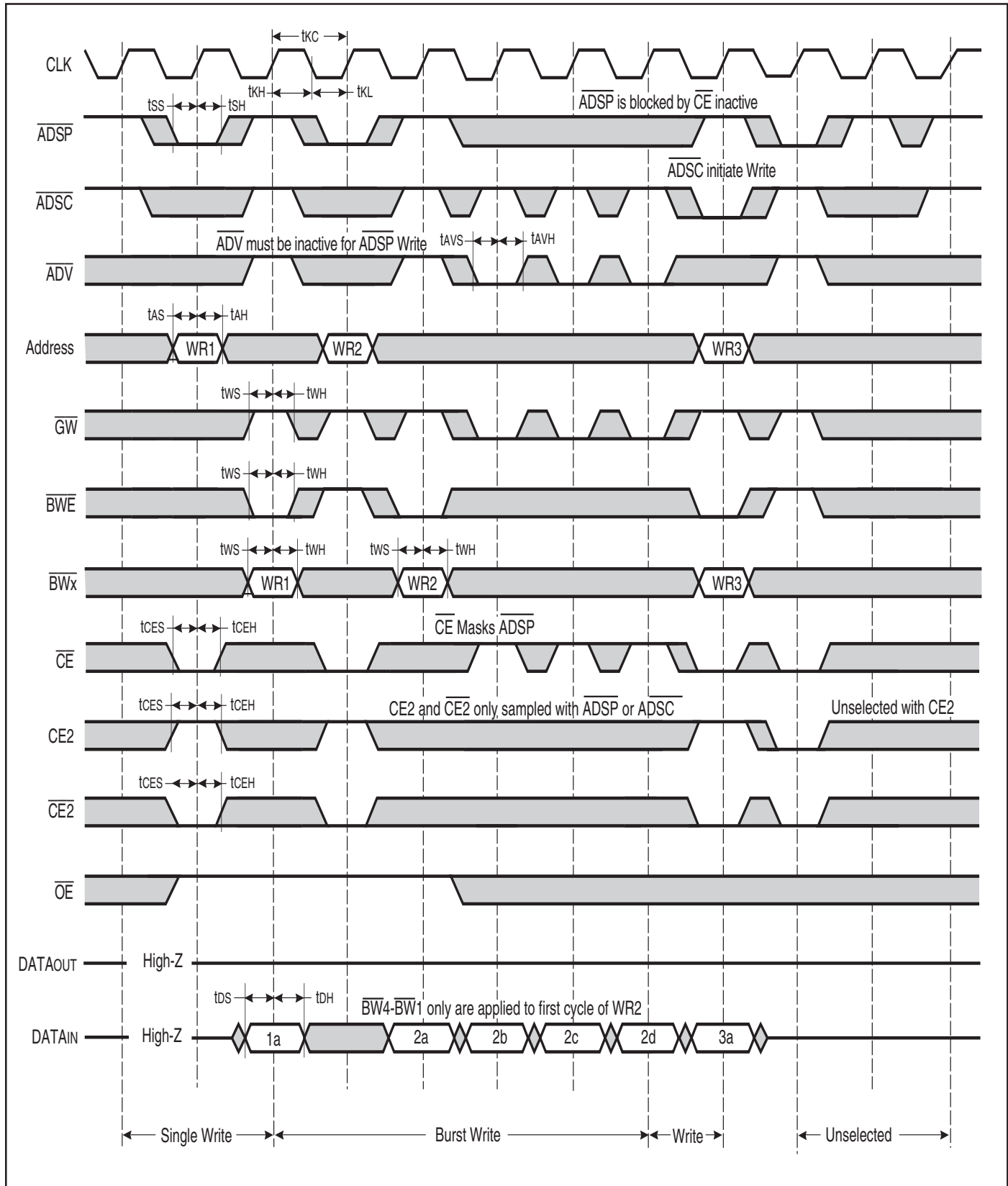
Note:

1. Configuration signal MODE is static and must not change during normal operation.
2. Guaranteed but not 100% tested. This parameter is periodically sampled.
3. Tested with load in Figure 2.

READ/WRITE CYCLE TIMING



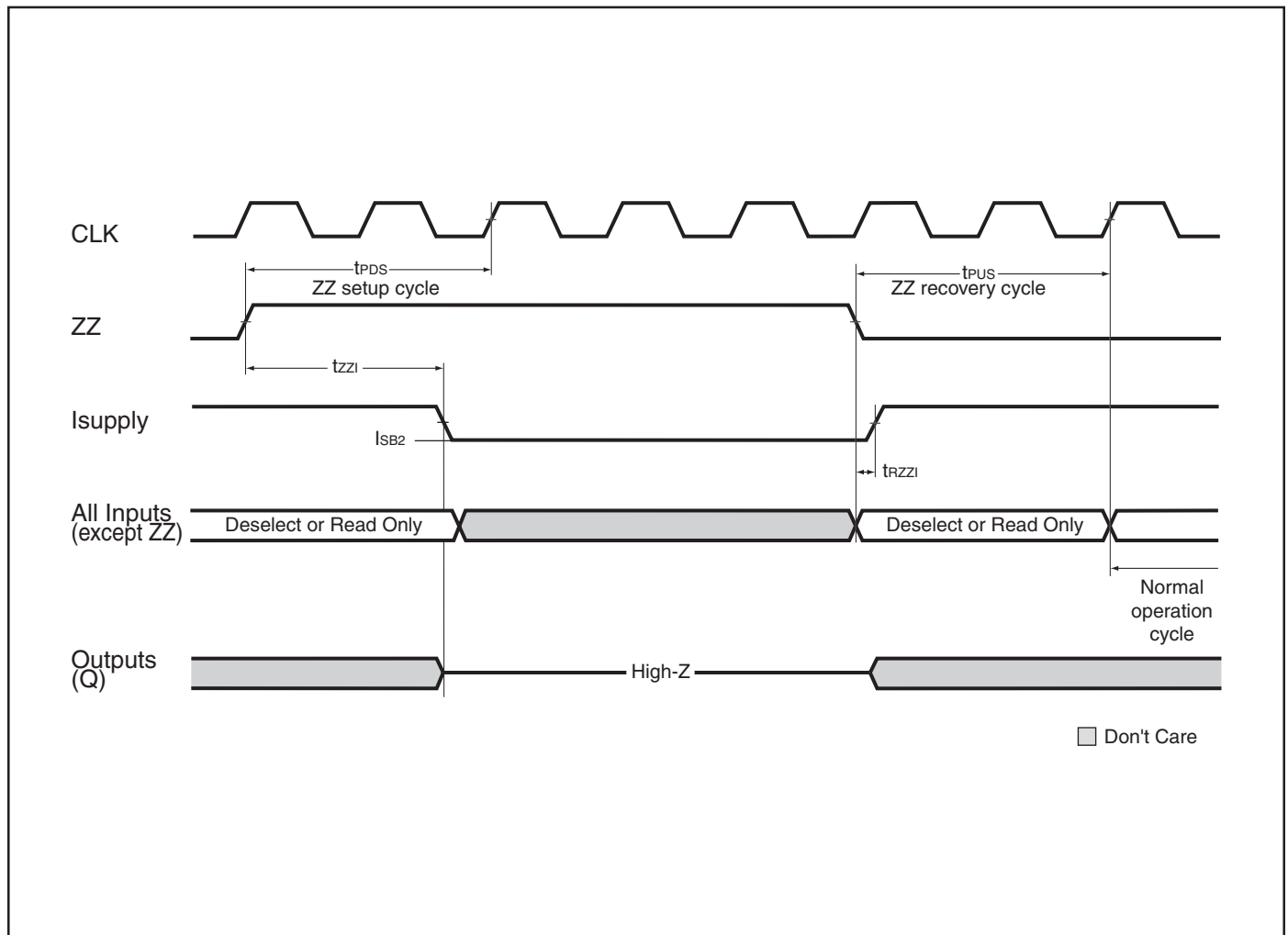
WRITE CYCLE TIMING



SNOOZE MODE ELECTRICAL CHARACTERISTICS

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|------------|------------------------------------|------------------|------|------|-------|
| I_{SB2} | Current during SNOOZE MODE | $ZZ \geq V_{ih}$ | — | 60 | mA |
| t_{PDS} | ZZ active to input ignored | | 2 | — | cycle |
| t_{PUS} | ZZ inactive to input sampled | | 2 | — | cycle |
| t_{ZZI} | ZZ active to SNOOZE current | | — | 2 | cycle |
| t_{RZZI} | ZZ inactive to exit SNOOZE current | | 0 | — | ns |

SNOOZE MODE TIMING





ORDERING INFORMATION (3.3V core/2.5V-3.3V I/O)

Commercial Range: 0°C to +70°C

| Configuration | Frequency | Order Part Number | Package |
|----------------|-----------|----------------------|---------------------|
| 128Kx32 | | | |
| | 250 | IS61LPS12832A-250TQ | 100 TQFP |
| | | IS61LPS12832A-250B2 | 119 PBGA |
| | | IS61LPS12832A-250B3 | 165 PBGA |
| | 200 | IS61LPS12832A-200TQ | 100 TQFP |
| | | IS61LPS12832A-200B2 | 119 PBGA |
| | | IS61LPS12832A-200B3 | 165 PBGA |
| 128Kx36 | | | |
| | 250 | IS61LPS12836A-250TQ | 100 TQFP |
| | | IS61LPS12836A-250TQL | 100 TQFP, Lead-free |
| | | IS61LPS12836A-250B2 | 119 PBGA |
| | | IS61LPS12836A-250B3 | 165 PBGA |
| | 200 | IS61LPS12836A-200TQ | 100 TQFP |
| | | IS61LPS12836A-200B2 | 119 PBGA |
| | | IS61LPS12836A-200B3 | 165 PBGA |
| 256Kx18 | | | |
| | 250 | IS61LPS25618A-250TQ | 100 TQFP |
| | | IS61LPS25618A-250B2 | 119 PBGA |
| | | IS61LPS25618A-250B3 | 165 PBGA |
| | 200 | IS61LPS25618A-200TQ | 100 TQFP |
| | | IS61LPS25618A-200B2 | 119 PBGA |
| | | IS61LPS25618A-200B3 | 165 PBGA |

ORDERING INFORMATION (3.3V core/2.5V-3.3V I/O)

Industrial Range: -40°C to +85°C

| Configuration | Frequency | Order Part Number | Package |
|----------------|-----------|-----------------------|---------------------|
| 128Kx32 | | | |
| | 250 | IS61LPS12832A-250TQI | 100 TQFP |
| | | IS61LPS12832A-250B2I | 119 PBGA |
| | | IS61LPS12832A-250B3I | 165 PBGA |
| | 200 | IS61LPS12832A-200TQI | 100 TQFP |
| | | IS61LPS12832A-200TQLI | 100 TQFP, Lead-free |
| | | IS61LPS12832A-200B2I | 119 PBGA |
| | | IS61LPS12832A-200B3I | 165 PBGA |
| 128Kx36 | | | |
| | 250 | IS61LPS12836A-250TQI | 100 TQFP |
| | | IS61LPS12836A-250B2I | 119 PBGA |
| | | IS61LPS12836A-250B3I | 165 PBGA |
| | 200 | IS61LPS12836A-200TQI | 100 TQFP |
| | | IS61LPS12836A-200TQLI | 100 TQFP, Lead-free |
| | | IS61LPS12836A-200B2I | 119 PBGA |
| | | IS61LPS12836A-200B2LI | 119 PBGA, Lead-free |
| | | IS61LPS12836A-200B3I | 165 PBGA |
| 256Kx18 | | | |
| | 250 | IS61LPS25618A-250TQI | 100 TQFP |
| | | IS61LPS25618A-250B2I | 119 PBGA |
| | | IS61LPS25618A-250B3I | 165 PBGA |
| | 200 | IS61LPS25618A-200TQI | 100 TQFP |
| | | IS61LPS25618A-200TQLI | 100 TQFP, Lead-free |
| | | IS61LPS25618A-200B2I | 119 PBGA |
| | | IS61LPS25618A-200B3I | 165 PBGA |

Automotive Range: -40°C to +125°C

| Configuration | Frequency | Order Part Number | Package |
|----------------|-----------|------------------------|---------------------|
| 128Kx32 | | | |
| | 200 | IS64LPS12832A-200TQA3 | 100 TQFP |
| | | IS64LPS12832A-200TQLA3 | 100 TQFP, Lead-free |
| 128Kx36 | | | |
| | 200 | IS64LPS12836A-200TQA3 | 100 TQFP |
| 256Kx18 | | | |
| | 200 | IS64LPS25618A-200TQA3 | 100 TQFP |

IS61(64)LPS12832A

IS61(64)LPS12836A IS61(64)VPS12836A

IS61(64)LPS25618A IS61(64)VPS25618A



ORDERING INFORMATION (2.5V core/2.5V I/O)

Commercial Range: 0°C to +70°C

| Configuration | Frequency | Order Part Number | Package |
|----------------|-----------|---------------------|----------|
| 128Kx36 | | | |
| | 250 | IS61VPS12836A-250TQ | 100 TQFP |
| | | IS61VPS12836A-250B2 | 119 PBGA |
| | | IS61VPS12836A-250B3 | 165 PBGA |
| | 200 | IS61VPS12836A-200TQ | 100 TQFP |
| | | IS61VPS12836A-200B2 | 119 PBGA |
| | | IS61VPS12836A-200B3 | 165 PBGA |
| 256Kx18 | | | |
| | 250 | IS61VPS25618A-250TQ | 100 TQFP |
| | | IS61VPS25618A-250B2 | 119 PBGA |
| | | IS61VPS25618A-250B3 | 165 PBGA |
| | 200 | IS61VPS25618A-200TQ | 100 TQFP |
| | | IS61VPS25618A-200B2 | 119 PBGA |
| | | IS61VPS25618A-200B3 | 165 PBGA |



Industrial Range: -40°C to +85°C

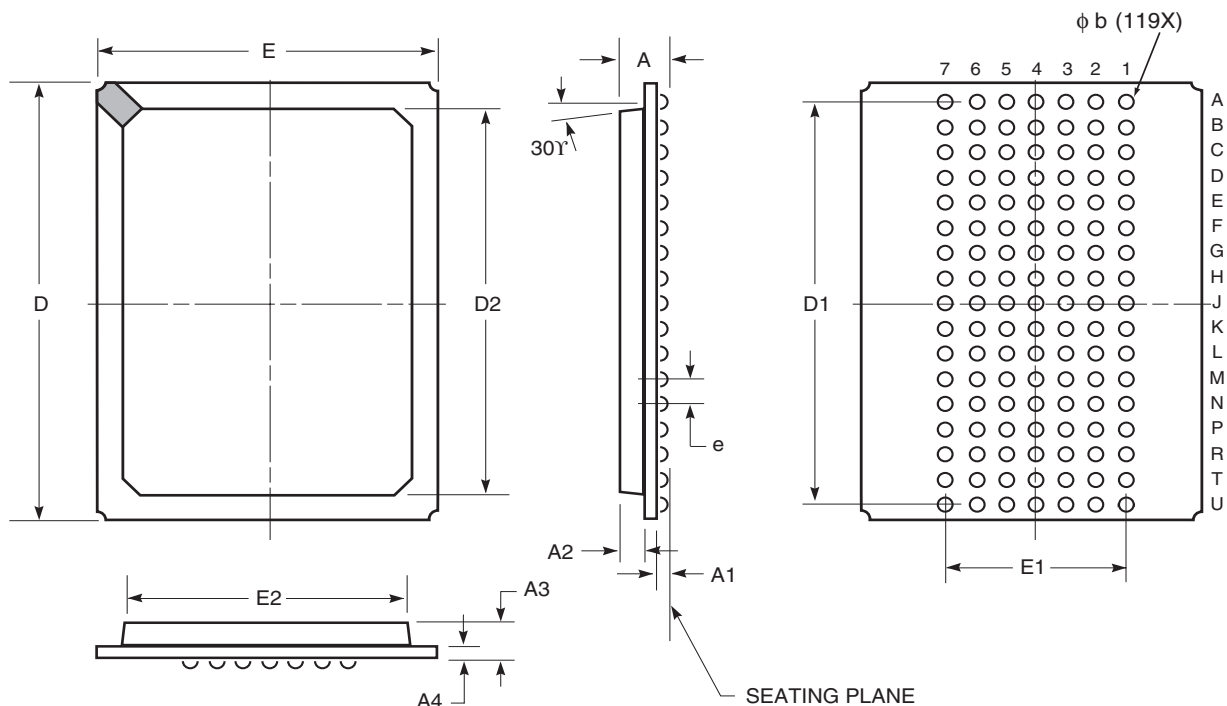
| Configuration | Frequency | Order Part Number | Package |
|----------------|-----------|----------------------|----------|
| 128Kx36 | | | |
| | 250 | IS61VPS12836A-250TQI | 100 TQFP |
| | | IS61VPS12836A-250B2I | 119 PBGA |
| | | IS61VPS12836A-250B3I | 165 PBGA |
| | 200 | IS61VPS12836A-200TQI | 100 TQFP |
| | | IS61VPS12836A-200B2I | 119 PBGA |
| | | IS61VPS12836A-200B3I | 165 PBGA |
| 256Kx18 | | | |
| | 250 | IS61VPS25618A-250TQI | 100 TQFP |
| | | IS61VPS25618A-250B2I | 119 PBGA |
| | | IS61VPS25618A-250B3I | 165 PBGA |
| | 200 | IS61VPS25618A-200TQI | 100 TQFP |
| | | IS61VPS25618A-200B2I | 119 PBGA |
| | | IS61VPS25618A-200B3I | 165 PBGA |

Automotive Range: -40°C to +125°C

| Configuration | Frequency | Order Part Number | Package |
|----------------|-----------|-----------------------|----------|
| 128Kx32 | | | |
| | 200 | IS64VPS12832A-200TQA3 | 100 TQFP |
| 128Kx36 | | | |
| | 200 | IS64VPS12836A-200TQA3 | 100 TQFP |
| 256Kx18 | | | |
| | 200 | IS64VPS25618A-200TQA3 | 100 TQFP |

PACKAGING INFORMATION

Plastic Ball Grid Array
 Package Code: B (119-pin)



| | MILLIMETERS | | INCHES | |
|--------------|-------------|-------|-----------|-------|
| Sym. | Min. | Max. | Min. | Max. |
| N0. Leads | 119 | | | |
| A | — | 2.41 | — | 0.095 |
| A1 | 0.50 | 0.70 | 0.020 | 0.028 |
| A2 | 0.80 | 1.00 | 0.032 | 0.039 |
| A3 | 1.30 | 1.70 | 0.051 | 0.067 |
| A4 | 0.56 BSC | | 0.022 BSC | |
| b | 0.60 | 0.90 | 0.024 | 0.035 |
| D | 21.80 | 22.20 | 0.858 | 0.874 |
| D1 | 20.32 BSC | | 0.800 BSC | |
| D2 | 19.40 | 19.60 | 0.764 | 0.772 |
| E | 13.80 | 14.20 | 0.543 | 0.559 |
| E1 | 7.62 BSC | | 0.300 BSC | |
| E2 | 11.90 | 12.10 | 0.469 | 0.476 |
| e | 1.27 BSC | | 0.050 BSC | |

Notes:

1. Controlling dimension: millimeters, unless otherwise specified.
2. BSC=Basic lead spacing between centers.
3. Dimensions D1 and E do not include mold flash protrusion and should be measured from the bottom of the package.
4. Formed leads shall be planar with respect to one another within 0.004 inches at the seating plane.

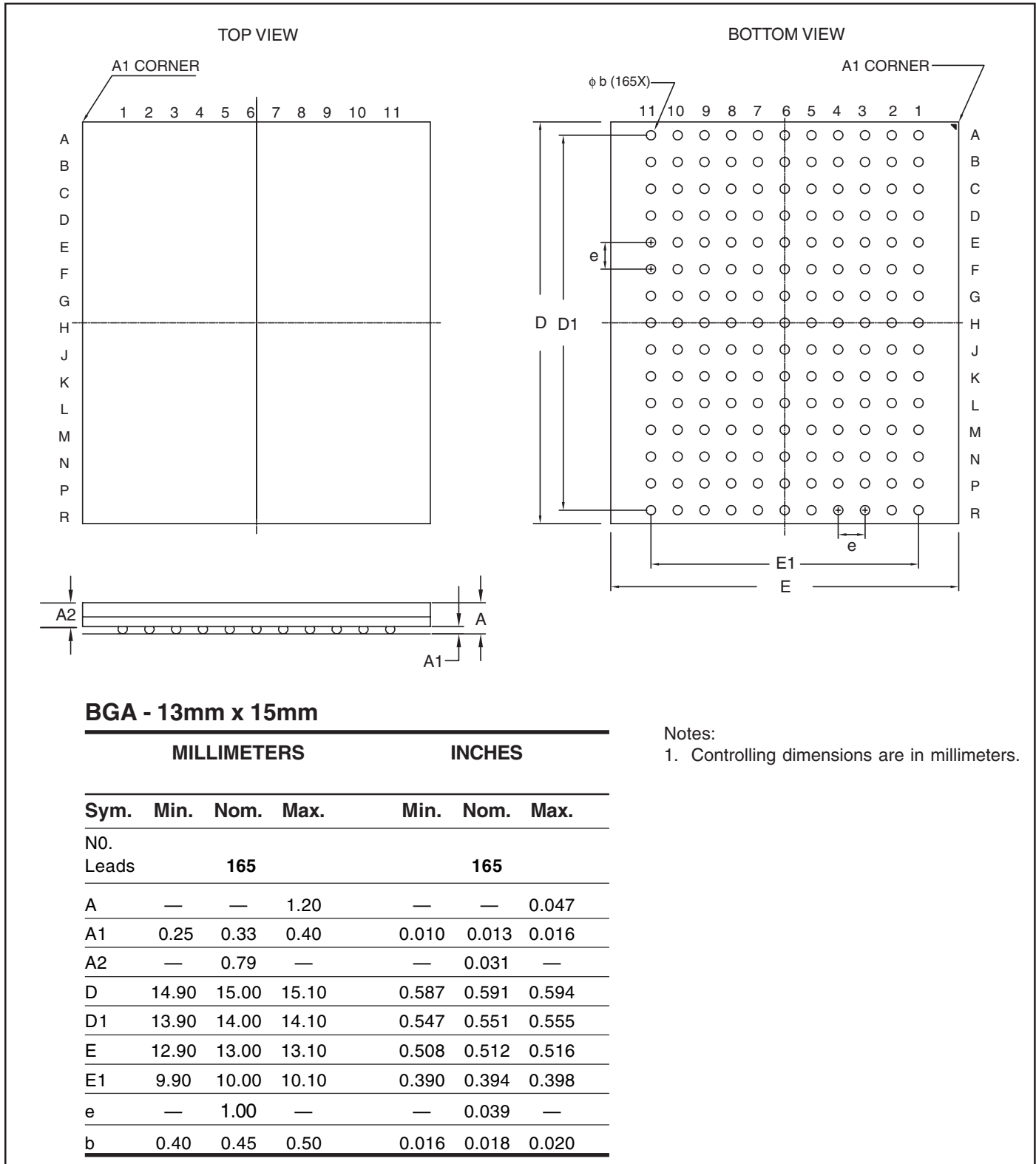
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 02/12/03

PACKAGING INFORMATION

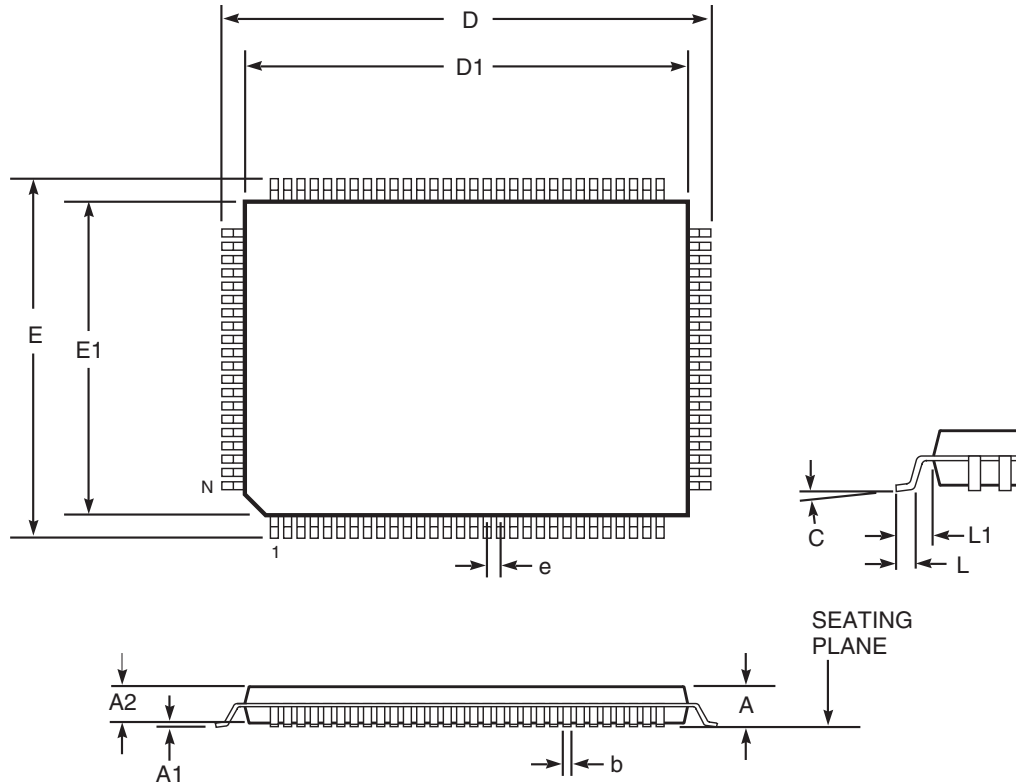
Ball Grid Array Package Code: B (165-pin)



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PACKAGING INFORMATION

TQFP (Thin Quad Flat Pack Package)
 Package Code: TQ



| Thin Quad Flat Pack (TQ) | | | | | | | | | |
|--------------------------|-------------|-------|------------|-------|-----------|-------------|------------|--------|-----|
| Symbol | Millimeters | | Inches | | Symbol | Millimeters | | Inches | |
| | Min | Max | Min | Max | | Min | Max | Min | Max |
| Ref. Std. | | | | | | | | | |
| No. Leads (N) | 100 | | | | 128 | | | | |
| A | — | 1.60 | — | 0.063 | — | 1.60 | — | 0.063 | |
| A1 | 0.05 | 0.15 | 0.002 | 0.006 | 0.05 | 0.15 | 0.002 | 0.006 | |
| A2 | 1.35 | 1.45 | 0.053 | 0.057 | 1.35 | 1.45 | 0.053 | 0.057 | |
| b | 0.22 | 0.38 | 0.009 | 0.015 | 0.17 | 0.27 | 0.007 | 0.011 | |
| D | 21.90 | 22.10 | 0.862 | 0.870 | 21.80 | 22.20 | 0.858 | 0.874 | |
| D1 | 19.90 | 20.10 | 0.783 | 0.791 | 19.90 | 20.10 | 0.783 | 0.791 | |
| E | 15.90 | 16.10 | 0.626 | 0.634 | 15.80 | 16.20 | 0.622 | 0.638 | |
| E1 | 13.90 | 14.10 | 0.547 | 0.555 | 13.90 | 14.10 | 0.547 | 0.555 | |
| e | 0.65 BSC | | 0.026 BSC | | 0.50 BSC | | 0.020 BSC | | |
| L | 0.45 | 0.75 | 0.018 | 0.030 | 0.45 | 0.75 | 0.018 | 0.030 | |
| L1 | 1.00 REF. | | 0.039 REF. | | 1.00 REF. | | 0.039 REF. | | |
| C | 0° | 7° | 0° | 7° | 0° | 7° | 0° | 7° | |

Notes:

1. All dimensioning and tolerancing conforms to ANSI Y14.5M-1982.
2. Dimensions D1 and E1 do not include mold protrusions. Allowable protrusion is 0.25 mm per side. D1 and E1 do include mold mismatch and are determined at datum plane -H-.
3. Controlling dimension: millimeters.